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Enhanced Drain Current of 4H-SiC MOSFETs by Adopting a Three-Dimensional Gate Structure

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***Abstract*—4H-SiC (0001) metal–oxide–semiconductor field-effect transistors (MOSFETs) with a 3-D gate structure, which has a top channel on the (0001) face and side-wall channels on the $\{11\bar{2}0\}$ face, have been fabricated. The 3-D gate structures with a 1–5-μm width and a 0.8-μm height have been formed by reactive ion etching, and the gate oxide has been deposited by plasma-enhanced chemical vapor deposition and then annealed in N_2O ambient at 1300 °C. The fabricated MOSFETs have exhibited good characteristics: The I_{ON}/I_{OFF} ratio, the subthreshold swing, and V_{TH} are 10^9, 210 mV/decade, and 3.5 V, respectively. The drain current normalized by the gate width is increasing with decreasing the gate width. The normalized drain current of a 1-μm-wide MOSFET is 16 times higher than that of a conventional planar MOSFET.**

***Index Terms*—Metal–oxide–semiconductor field-effect transistor (MOSFET), multigate FET (MuGFET), silicon carbide (SiC), 3-D gate structure.**

I. Introduction

SILICON CARBIDE metal–oxide–semiconductor field-effect transistors (SiC MOSFETs) have attracted much attention as low-loss power MOSFETs as well as devices of integrated circuits for high-temperature use [1]. However, SiC MOSFETs have still suffered from low channel mobility and, thereby, low drain current due to the high interface state density of SiO_2/SiC. In order to increase the drain current, several approaches can be considered. First, increasing the channel mobility has been intensively investigated by many groups. For example, oxidation or reoxidation in NO or N_2O ambient is an attractive process to improve the inversion channel mobility [2], [3]. Oxidation or reoxidation in pyrogenic atmosphere is also an effective process to increase the inversion channel mobility [4]. The utilization of the $\{11\bar{2}0\}$ face [5] or $(000\bar{1})$ face [6] is another attractive approach to obtain a high channel mobility. Second, reducing the channel length is also effective to enhance the drain current [7], [8]. The third method is to increase the gate capacitance either by reducing the thickness of the gate oxide or by using the high-κ material as the gate insulator [9].

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Another method to enhance the drain current is to increase the channel width. In advanced Si MOSFETs, MOSFETs with multigate structures have been extensively developed in order to increase the ON-current while minimizing the short-channel effects [10], [11]. In short-channel multigate MOSFETs, the influence of the drain potential on the channel is reduced because the electric field from the drain is effectively terminated by the multigates. The drain current of a multigate MOSFET is the sum of currents flowing along all the interfaces covered by the gate electrode. Therefore, the current of a multigate MOSFET is much higher than that of a conventional planar MOSFET with a given channel area, owing to the large effective channel width. When a 3-D gate structure is adopted to SiC (0001) MOSFETs, the drain current will be further enhanced due to the anisotropy of the inversion channel mobility; a high channel mobility on the $\{11\bar{2}0\}$ sidewalls will enhance the drain current. The multigate structure can be applied to SiC power MOS devices with a lateral channel, such as double-implanted MOSFETs (DMOSFETs) and reduced surface field (RESURF) MOSFETs. In these devices, the channel with the multigate structure is not always formed in the high electric field regions. The short-channel SiC complementary MOS devices are another application of the multigate structure in the future.

In this paper, the authors have fabricated 4H-SiC (0001) MOSFETs with a 3-D gate structure with a 0.8-μm height, a 1–5-μm width, and a 5–10-μm channel length. The fabricated devices showed good characteristics, and the 3-D gate structure MOSFET with the $\{11\bar{2}0\}$ sidewall exhibited 16 times higher drain current than a conventional planar MOSFET. The mobility on the $\{11\bar{2}0\}$ sidewall was estimated to be 42 $cm^2/V \cdot s$.

II. Device Fabrication

The schematic illustrations of a MOSFET with a 3-D gate structure employed in this paper are shown in Fig. 1(a) and (b). The height of the gate structure (H) was fixed at 0.8 μm, the width (W) was varied from 1 to 5 μm, and the channel length (L) was varied from 5 to 10 μm. The sidewall plane of the 3-D gate structure is either the $\{11\bar{2}0\}$ face or the $\{1\bar{1}00\}$ face, which is vertical to the $\{11\bar{2}0\}$ face. The depth of the n^+ region (source/drain) is 0.8 μm $(= H)$ to ensure that the current flows along the sidewall channels. By forming the p^+ region in the bottom plane, the threshold voltage of the bottom channel was significantly increased, so that the drain current flowing along the 3-D gate structure can be evaluated. When a gate oxide is formed by thermal oxidation, the oxide thickness on

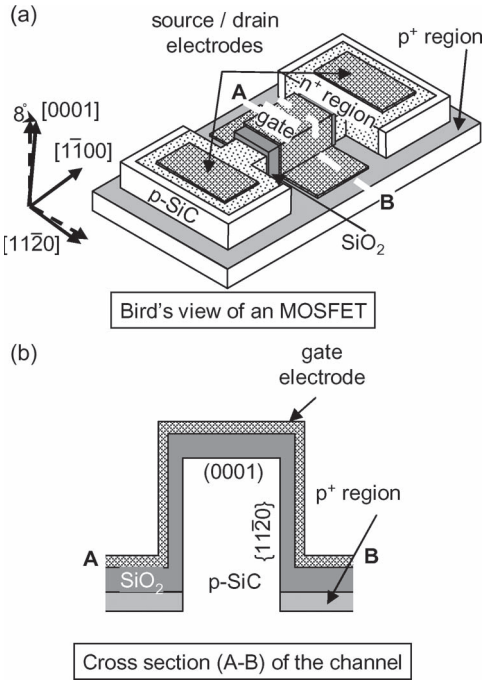

Fig. 1. Schematic illustrations of an SiC 3-D gate structure MOSFET. (a) Bird's-eye view of the MOSFET. (b) Cross section of channel region.

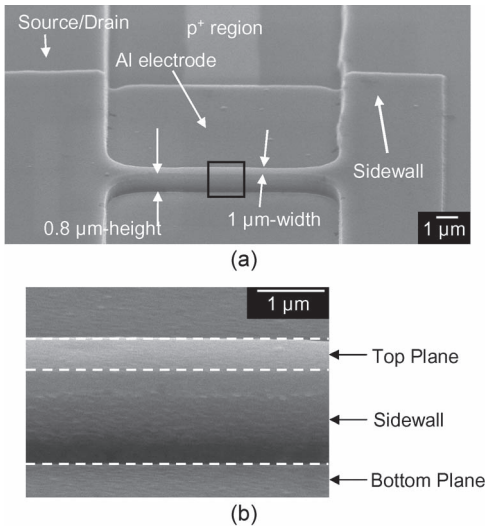

Fig. 2. (a) Scanning electron microscopy image of the fabricated 4H-SiC (0001) MOSFET with a 3-D gate structure. (b) Magnified image of the sidewall channel region indicated by a square in (a).

the sidewalls becomes larger than that on the top plane due to the oxidation rate anisotropy of SiC [12]. The thick oxide on the sidewalls results in high threshold voltage and low drain current on the sidewall channels. In order to obtain a thinner gate oxide on the sidewalls than that on the top plane, the gate oxide was formed by plasma-enhanced chemical vapor deposition (PECVD), as described hereafter. The MOSFETs with a 3-D gate structure were fabricated on a p-type 8° off-axis 4H-SiC (0001) epilayer. The thickness and the acceptor concentration of the epilayer was 10 μm and 7.8×10^{15} cm^{-3}, respectively. The relatively deep (0.8 μm) source and drain regions were formed by multiple N^+ implantation (80–700 keV with total dose of 1.0×10^{15} cm^{-2} at 200 °C), combined with high-dose P^+ implantation (10–110 keV with 5.0×10^{15} cm^{-2} at 300 °C) into the surface region in order to minimize the contact resistance. A 2-μm-thick SiO_2 deposited by PECVD was employed as an implantation mask. The 3-D structures with a 0.8-μm height and a 1–5-μm width were formed by reactive ion etching (RIE) with a 1-μm-thick SiO_2 mask. Subsequently, Al^+ ions were implanted to form the bottom p^+ region with the same SiO_2 mask. After covering the sample with a carbon cap [13], the implanted dopants were activated in Ar ambient at 1700 °C for 30 min. In order to reduce the damage induced by RIE, sacrificial oxidation at 1100 °C for 1 h was performed. After depositing SiO_2 as a gate oxide by PECVD, N_2O annealing at 1300 °C for 30 min was carried out to reduce the SiO_2/SiC interface state density [14]. The thickness of the deposited oxide is 70 nm on the top plane and 45 nm on the sidewall plane, as determined by cross-sectional scanning electron microscopy. Ni was deposited and annealed at 950 °C for 10 min as ohmic contacts on the source and drain. Al was employed as a gate electrode.

Fig. 2 shows the scanning electron microscopy image of a fabricated MOSFET with a 1-μm-wide 3-D gate structure. As shown in the figure, the sidewall plane is flat and nearly vertical to the bottom plane. The gate electrode covers not only the 3-D gate structure but also the edges of source and drain regions, although the electrode covers only the 3-D gate structure in Fig. 1 for simplicity.

To investigate the effect of the 3-D gate structure, a planar MOSFET was also fabricated on the same chip.

III. Results and Discussions

Fig. 3(a) and (b) shows the drain characteristics of fabricated 3-D gate MOSFETs with the $\{11\bar{2}0\}$ sidewalls (a) and $\{1\bar{1}00\}$ sidewalls (b), respectively. The channel length and gate width of the MOSFETs are 5 and 1 μm, respectively. Both of the figures show good characteristics as a MOSFET, and the gate leakage current was very low, i.e., in the 1–100-pA range. The drain current of the MOSFET with the $\{11\bar{2}0\}$ sidewalls is higher than that with the $\{1\bar{1}00\}$ sidewalls. This can be attributed to higher channel mobility on the $\{11\bar{2}0\}$ sidewalls than that on the $\{1\bar{1}00\}$ sidewalls.

Fig. 4(a) shows the gate characteristics of the MOSFETs with the $\{11\bar{2}0\}$ and $\{1\bar{1}00\}$ sidewalls, as well as that of a conventional planar MOSFET in the linear region ($V_D = 0.1$ V). Here, the drain current is normalized by the double of the gate width ($2W$), while that of the planar MOSFET is normalized by the gate width (W). Since the 3-D gate structure will be repeated in parallel to increase the total drain current in real devices, the drain current was normalized by not W but $2W$, assuming a periodic 3-D gate structure with a projected gate width of W and a spacing of W (period: $2W$). The drain current of the 1-μm-wide gate MOSFET with the $\{11\bar{2}0\}$ sidewalls is about 16 times higher than that of the planar MOSFET at $V_G = 12$ V. Fig. 4(b) shows the subthreshold characteristics in the linear region. As shown in the figure, all the fabricated MOSFETs exhibited good ON-/OFF-current ratio and subthreshold swing.

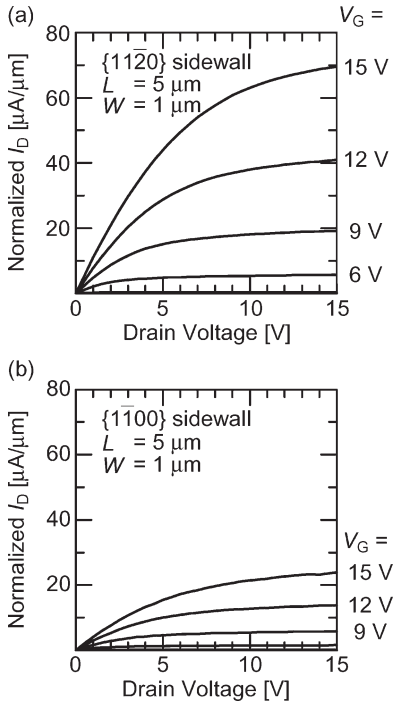

Fig. 3. Drain characteristics of 3-D gate structure MOSFETs (a) with the $\{11\bar{2}0\}$ and (b) $\{1\bar{1}00\}$ sidewalls. The gate voltage was varied from 0 to 15 V with a 3-V step.

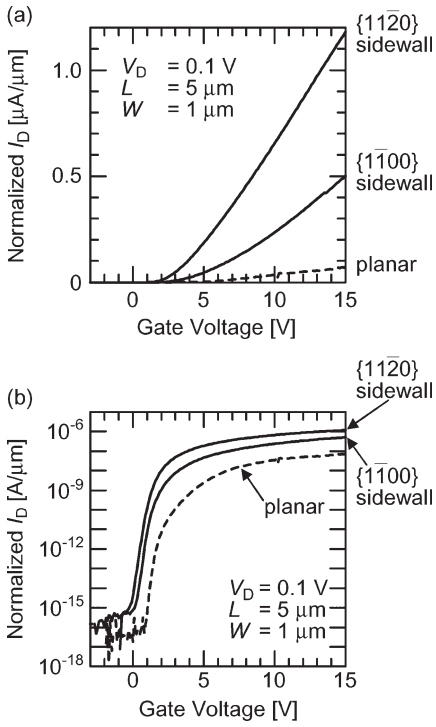

Fig. 4. (a) Gate and (b) subthreshold characteristics of 3-D gate structure MOSFETs with the $\{11\bar{2}0\}$ and $\{1\bar{1}00\}$ sidewalls and conventional planar MOSFET. The drain current of the 3-D gate MOSFET is normalized by the double of the gate width $(2W)$, while that of planar MOSFET is normalized by the gate width (W).

Table I summarizes the normalized drain current $(I_D/2W)$ at $V_G = 12$ V and $V_D = 0.1$ V, threshold voltage $(V_{\rm TH})$, the subthreshold swing (S), the ratio of the ON-/OFF-current $(I_{\rm ON}/I_{\rm OFF})$ of the 1-μm-wide and 5-μm-long 3-D gate MOSFETs with the $\{11\bar{2}0\}$ and $\{1\bar{1}00\}$ sidewalls, and those of a planar MOSFET.

TABLE I
CHARACTERISTICS OF THE FABRICATED 1-μm-WIDE AND 5-μm-LONG 3-D GATE MOSFETs WITH THE $\{11\bar{2}0\}$ AND $\{1\bar{1}00\}$ SIDEWALLS, WHILE THOSE OF THE PLANAR MOSFET ARE ALSO SHOWN. THE NORMALIZED DRAIN CURRENT $(I_D/2W)$ AT $V_G = 12$ V AND $V_D = 0.1$ V, THRESHOLD VOLTAGE $(V_{\rm TH})$, SUBTHRESHOLD SWING (S), AND RATIO OF ON-/OFF-CURRENT $(I_{\rm ON}/I_{\rm OFF})$ ARE SUMMARIZED

	$I_D/2W$ [μA/μm]	$V_{\rm TH}$ [V]	S [mV/decade]	$I_{\rm ON}/I_{\rm OFF}$
$\{11\bar{2}0\}$ sidewall MOSFET	0.86	3.4	209	10^9
$\{1\bar{1}00\}$ sidewall MOSFET	0.34	4.8	201	10^9
planar MOSFET	0.05 (I_D/W)	5.3	177	10^8

The subthreshold swing (S) obtained from the MOSFETs fabricated in this paper is rather good, 177–209 mV/decade, compared with previous reports (220–471 mV/decade) [15]–[17].

The subthreshold swings (S) of the 3-D gate MOSFETs are about 30 mV/decade higher than that of the planar MOSFET. This may be caused by a relatively high interface state density in the energetically deep region for SiO_2/SiC $\{11\bar{2}0\}$ and $\{1\bar{1}00\}$ [18]. The threshold voltage of the MOSFET with the $\{11\bar{2}0\}$ and $\{1\bar{1}00\}$ sidewalls and that of the planar MOSFET is 3.5, 4.8, and 5.3 V, respectively. The threshold voltage of the $\{11\bar{2}0\}$ sidewall MOSFET is about 1.5 V smaller than that of the planar MOSFET. This can be due to the thinner oxide thickness on the sidewall planes than that for the planar MOSFET. The threshold voltage of the $\{11\bar{2}0\}$ sidewall MOSFET is also smaller than that of the $\{1\bar{1}00\}$ MOSFET. This can originate from the lower interface state density of SiO_2/4H-SiC $\{11\bar{2}0\}$ near the conduction band edge than that of SiO_2/4H-SiC $\{1\bar{1}00\}$ because the threshold voltage is evaluated from the linear extrapolation in the gate characteristics [Fig. 4(a)].

Fig. 5(a) and (b) shows the gate characteristics of 10-μm-long 3-D gate MOSFETs with various gate widths with the $\{11\bar{2}0\}$ sidewalls (a) and with the $\{1\bar{1}00\}$ sidewalls (b), respectively. As shown in both panels, the normalized drain current increases with decreasing the gate width. This indicates that the geometric effects, forming the inversion channel on the sidewall planes, are effective to increase the drain current per channel area. However, the effects of the high channel mobility on sidewall planes cannot be readily addressed from this result.

The authors tried to estimate the channel mobility on the sidewall channels with simple equations as described next.

The drain current of a 3-D gate MOSFET in the linear region can be written as

$$\begin{aligned} I_D &= I_{D(\rm top)} + 2I_{D(\rm side)} \\ &= \mu_{\rm top}\frac{W}{L}C_{\rm ox(top)}\left(V_G - V_{\rm TH(top)}\right)V_D \\ &\quad + 2\mu_{\rm side}\frac{H}{L}C_{\rm ox(side)}\left(V_G - V_{\rm TH(side)}\right)V_D \end{aligned} \quad (1)$$

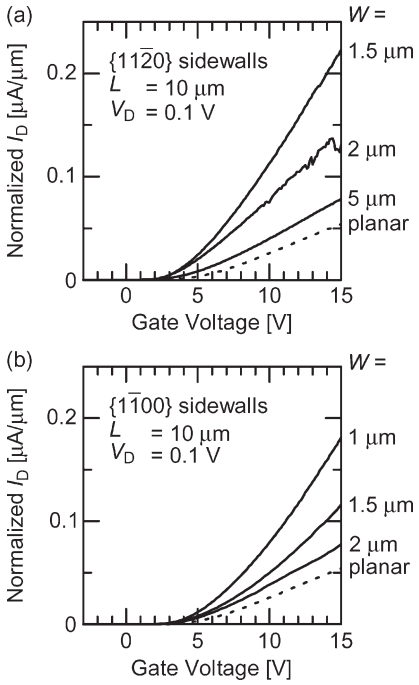

Fig. 5. Gate characteristics of 5-μm-long 3-D gate MOSFETs with various gate widths with the (a) $\{11\bar{2}0\}$ and (b) $\{1\bar{1}00\}$ sidewalls.

where $I_{D(\mathrm{top})}$ and $I_{D(\mathrm{side})}$ are the drain current flowing in the top channel and in the sidewall channels, μ_{top} and μ_{side} are the inversion channel mobility in the top channel and in the sidewall channels, $V_{\mathrm{TH(top)}}$ and $V_{\mathrm{TH(side)}}$ are the threshold voltage in the top channel (5.3 V) and in the sidewall channels (3.4 V), and $C_{\mathrm{ox(top)}}$ and $C_{\mathrm{ox(side)}}$ are the gate capacitance per unit area of the top plane (4.9×10^{-8} F/cm^2) and of the sidewall planes (7.6×10^{-8} F/cm^2), respectively. W, H, and L are the width, the height (0.8 μm), and the channel length (10 μm) of the 3-D gate structure, respectively. V_G and V_D are the gate (12 V) and drain voltage (0.1 V), respectively. The $I_{D(\mathrm{side})}$ can be expressed as

$$I_{D(\mathrm{side})} = I_{D(\mathrm{top})} \cdot \frac{\mu_{\mathrm{side}}}{\mu_{\mathrm{top}}} \frac{H}{W} \frac{C_{\mathrm{ox(side)}}}{C_{\mathrm{ox(top)}}} \frac{V_g - V_{\mathrm{TH(side)}}}{V_g - V_{\mathrm{TH(top)}}}. \quad (2)$$

Substituting (2) into (1), the drain current normalized by the double of the gate width ($I_D/2W$) can be expressed as

$$\frac{I_D}{2W} = \frac{I_{D(\mathrm{top})}}{W} \left(\frac{1}{2} + \frac{\mu_{\mathrm{side}}}{\mu_{\mathrm{top}}} \frac{H}{W} \frac{C_{\mathrm{ox(side)}}}{C_{\mathrm{ox(top)}}} \frac{V_g - V_{\mathrm{TH(side)}}}{V_g - V_{\mathrm{TH(top)}}} \right). \quad (3)$$

All the parameters in (3) are known except for $I_{D(\mathrm{top})}$ and $\mu_{\mathrm{side}}/\mu_{\mathrm{top}}$. By using the normalized drain current of the planar MOSFET ($I_{D\,\mathrm{planar}}/W_{\mathrm{planar}}$) as $I_{D(\mathrm{top})}/W$, $I_D/2W$ can be calculated by assuming the only unknown parameter $R = \mu_{\mathrm{side}}/\mu_{\mathrm{top}}$.

Fig. 6 shows the dependence of the normalized drain current on the gate width at $V_G = 12$ V and $V_D = 0.1$ V. The open and closed symbols indicate the experimental results obtained from the $\{11\bar{2}0\}$ sidewall MOSFETs and the $\{1\bar{1}00\}$ sidewall MOSFETs, respectively. The dotted lines denote the dependence calculated for the mobility ratio $R = \mu_{\mathrm{top}}/\mu_{\mathrm{side}} = 1, 1.5, 3$ by using (3), where the $I_{D(\mathrm{top})}/W$ value was determined from the characteristics of the planar MOSFET. The closed symbols ($\{1\bar{1}00\}$ sidewall MOSFETs) and open symbols ($\{11\bar{2}0\}$ sidewall MOSFETs) show reasonable agreement with the line simulated for $R = 1.5$ and $R = 3$, respectively. The inversion channel mobility in the top channel was determined as 14 cm^2/Vs from the characteristics of the planar MOSFET. Then, the inversion channel mobility on the $\{11\bar{2}0\}$ and $\{1\bar{1}00\}$ sidewalls can be estimated to be 42 and 21 cm^2/Vs, respectively.

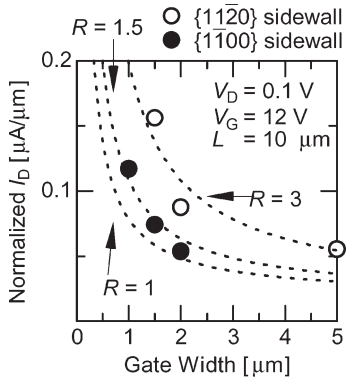

Fig. 6. Dependence of the normalized drain current on the gate width at $V_G = 12$ V and $V_D = 0.1$ V. The open and closed symbols denote the experimental results for the $\{11\bar{2}0\}$ and $\{1\bar{1}00\}$ sidewall MOSFET, respectively. The dotted lines show the dependence calculated for the mobility ratio $R = \mu_{\mathrm{side}}/\mu_{\mathrm{top}} = 1, 1.5, 3$ by using the characteristics of the planar MOSFET.

Thus, the 3-D gate structure MOSFETs are attractive for increasing the drain current of SiC MOSFETs. The major disadvantages include the increased input capacitance and possibly increased gate leakage.

As the MOSFETs were fabricated on a 4H-SiC (0001) wafer 8° inclined toward the $[11\bar{2}0]$ direction, the $\{11\bar{2}0\}$ sidewalls are apart from the exact $(11\bar{2}0)$ face. The evaluated mobility of the sidewalls is the average mobility of the two sidewall channels. Although their oxide-forming process is different from that of this paper, Yano *et al.* have investigated the mobility of a trench MOSFET which has a single sidewall channel on the $\{11\bar{2}0\}$, $\{\bar{1}\bar{1}20\}$, $\{1\bar{1}00\}$, and $\{\bar{1}100\}$ faces, where the oxides were formed by wet oxidation at 1150 °C for 150 min and followed by wet reoxidation anneal at 750 °C for 180 min, and NO annealing at 1150 °C for 60 min was also carried out [19]. They reported that the mobility on the $\{1\bar{1}00\}$ and $\{\bar{1}100\}$ faces is 32 and 35 cm^2/V · s, respectively. These mobilities are higher than that of the $\{1\bar{1}00\}$ sidewall MOSFET fabricated in this paper. On the other hand, they estimated the mobility on the $\{11\bar{2}0\}$ and $\{\bar{1}\bar{1}20\}$ faces as 43 and 21 cm^2/V · s, respectively, which are similar to that of the $\{11\bar{2}0\}$ sidewall MOSFET fabricated in this paper. The difference of the mobility values may originate from the difference of the taper of the sidewalls and/or the formation process of the gate oxides. In fact, the mobility in the accurate $(11\bar{2}0)$ and $(\bar{1}\bar{1}20)$ sidewall channels has been estimated to be 72 and 66 cm^2/V · s by the same group, respectively [20].

IV. Conclusion

Some 4H-SiC (0001) MOSFETs with a 3-D gate structure have been fabricated and electrically characterized. The

3-D structures, which have flat sidewalls nearly vertical to the bottom plane, were formed by RIE. The sidewall plane of the gate structure is either $\{11\bar{2}0\}$ or $\{1\bar{1}00\}$. The drain current normalized by the gate width increased with decreasing the gate width, and the normalized drain current of the 1-μm-wide MOSFET with the $\{11\bar{2}0\}$ sidewalls was about 16 times higher than that of a planar MOSFET. This improvement of the drain current originates from both the geometrical effects and the high inversion channel mobility on the $\{11\bar{2}0\}$ sidewalls. The inversion channel mobility on the $\{11\bar{2}0\}$ sidewall channels was estimated to be 42 $\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$.

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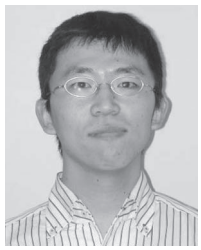

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